

EEL3701

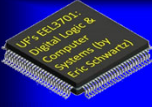
Menu

- More MSI elements
 - > Open collector gates



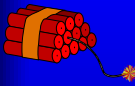
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A No-No!



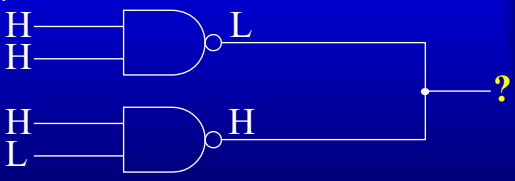
DO NOT DO THIS IN LAB !!!!



- **Question:** What if we connect:

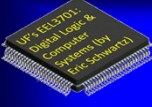
H
H

H
L


- **Answer:** 
 - Why? _____

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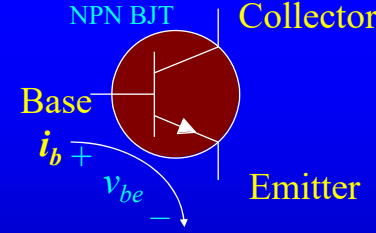
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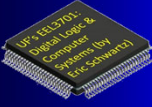
Transistor-Transistor Logic

- TTL $\equiv$ Transistor-Transistor Logic
- A transistor looks like a current controlled switch.
- When there is a voltage across the base-emitter ($v_{be} > 0$), there is a current i_b .
- When $i_b > 0$, the transistor conducts, and the collector to emitter junction looks like a wire (**short circuit**).
- When $i_b \cong 0$, the transistor does **not** conduct, and the collector to emitter junction looks like an **open circuit**.



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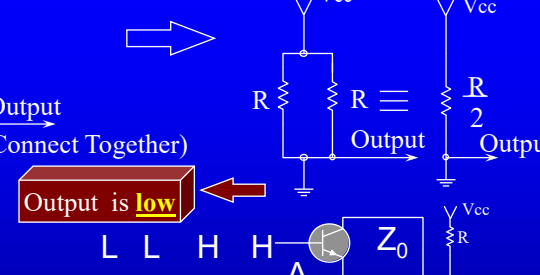


EEL3701 Open Collector (O.C.) Gates

If any of the transistors conducts, i.e., if **any input is H**:

Input Combinations

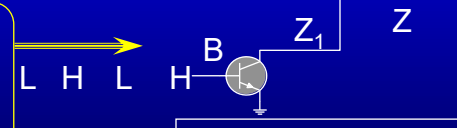
L	L	H	H
L	H	L	H



Output (Connect Together)

Output is low

Now suppose you leave off the resistor R from the collector in the circuit. This is called an **Open Collector (O.C.) gate**.



If Z_0 & Z_1 & Z are not connected & are all active-low, $\Rightarrow Z = Z_0 + Z_1$

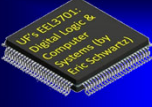
$Z = H$ only if $A=B=L$, i.e., $Z = A * B$, where $Z(H), A(L), B(L)$



$Z = A * B = 1 / (1/A + 1/B)$

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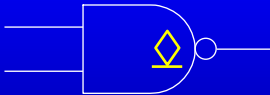
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Symbols for Open Collector

- Open Collector 2-input NAND gate (74'03)



OC



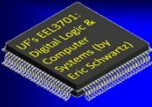
IEEE Symbol



Our Symbol

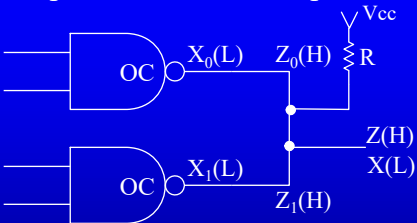
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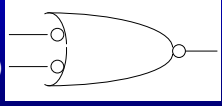
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Open Collector Gate

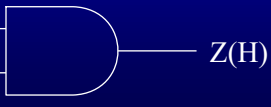
- A simple representation of an Open Collector Gate is:



- Q: What is X.L?
- A: **Wired "OR"** $X = X_1 + X_0$
- Q: What is Z.H ?
- A: **Wired "AND"** $Z = Z_1 \cdot Z_0$



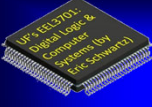
$X_0(L)$
 $X_1(L)$ → $X(L)$



$Z_0(H)$
 $Z_1(H)$ → $Z(H)$

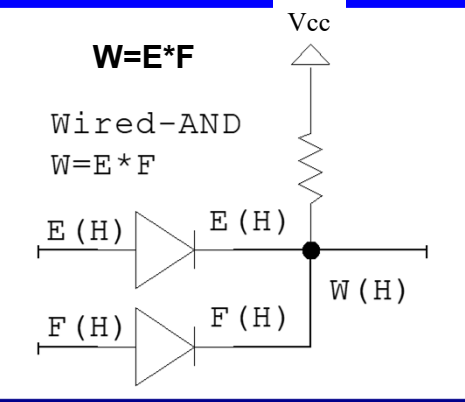
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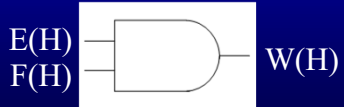
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Open Collector Bus

- Open collector bus connection
 - > Wired-AND
- Example (wired-OR):
 - > Using LW's: *Buffer-1 O.C.*
 - > 74'07
- Go to LogicWorks for proof

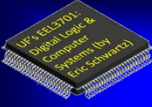


W=E*F
Wired-AND
 $W=E * F$



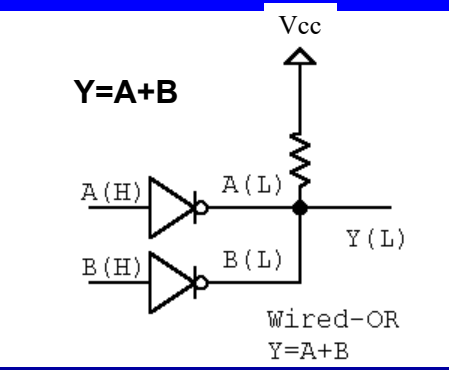
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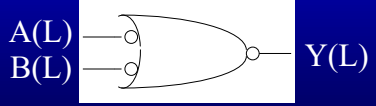
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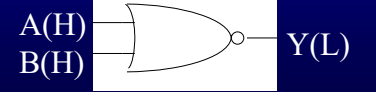
Open Collector Bus

- Open collector bus connection
 - > Wired-OR
 - > Wired-AND
- Example (wired-OR):
 - > Using LW's: *NOT O.C.*
 - > 74'05
- Go to LogicWorks for proof



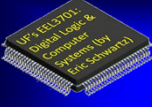
Y=A+B
Wired-OR
 $Y=A+B$





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Open Collector Bus

- Example (wired-AND):
- Go to LogicWorks for proof
 - > I made this symbol in LW:
 - NOT O.C. (Active-low In)**
 - > 74'05

$X = C * D$

Wired-AND
 $X = C * D$

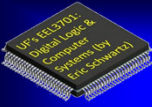
$C(H)$
 $D(H)$
 $X(H)$

$C(L)$
 $D(L)$
 $X(H)$

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Wired-AND, OR.cct

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Open Collector Example

- Find Y and X
- Compare Y to X $Y = /X$

$Y = /AB * /(C + /D)$
 $Y = /AB /CD$

$A(L)$
 $B(H)$
 $C(H)$
 $D(L)$
 $Y(H)$

$X = /(/AB) + (C + /D)$
 $X = A + /B + C + /D$

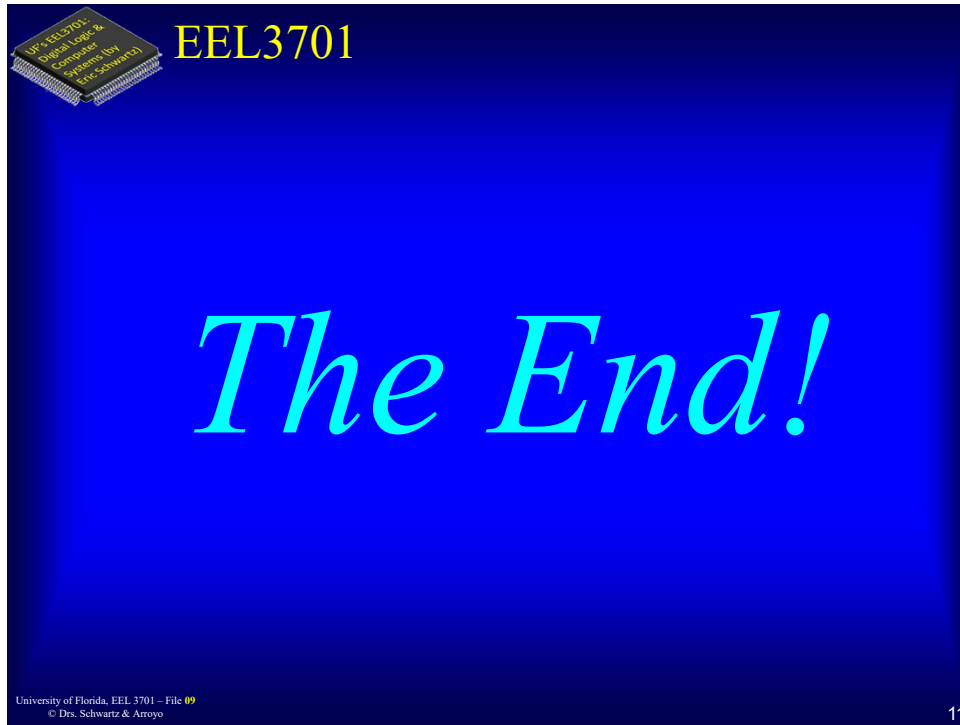
$A(L)$
 $B(H)$
 $C(H)$
 $D(L)$
 $X(L)$

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OC_example.cct

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Digital Logic &
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The End!

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